

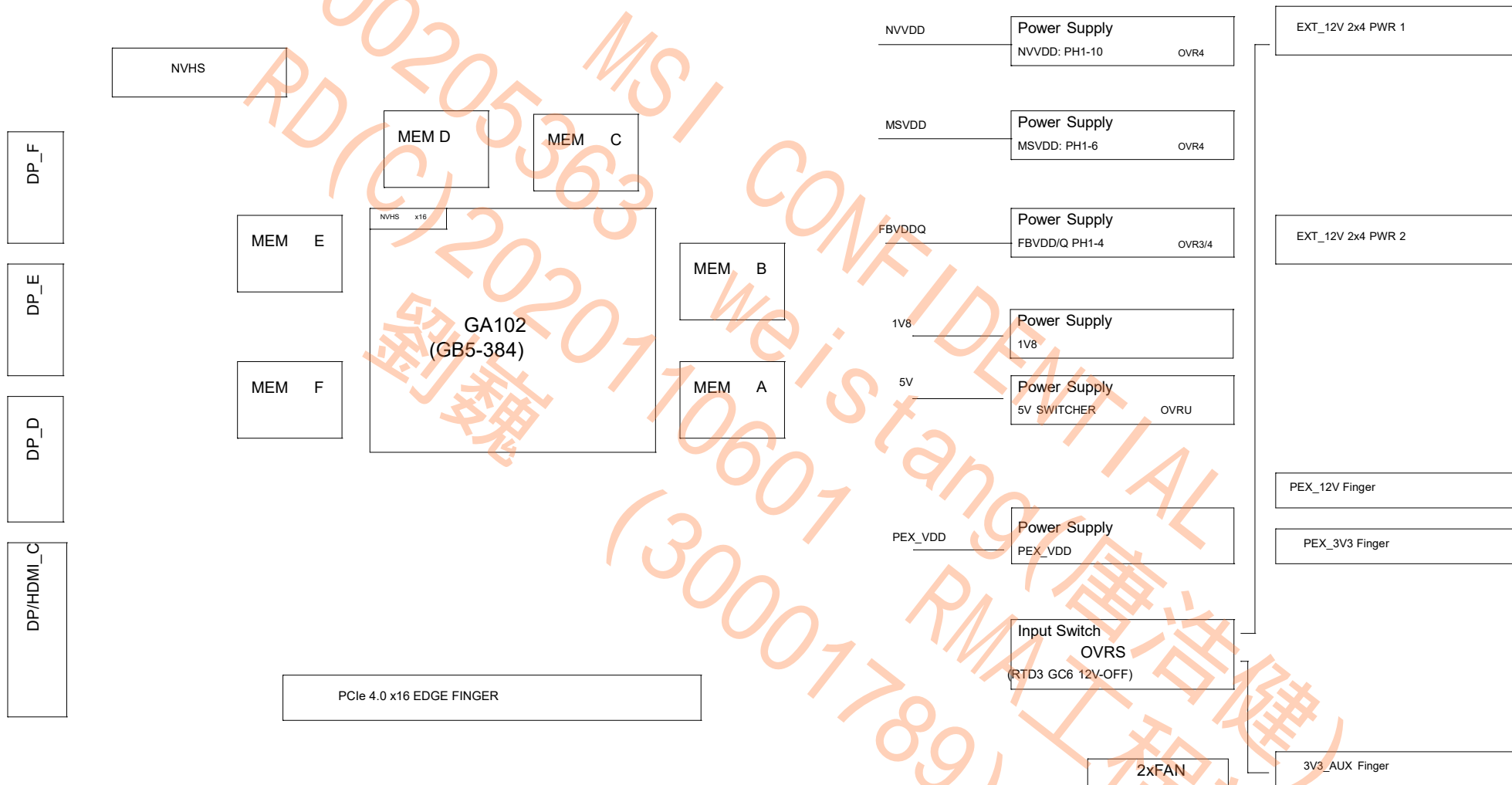
GA102 DT SKU P-BOARD

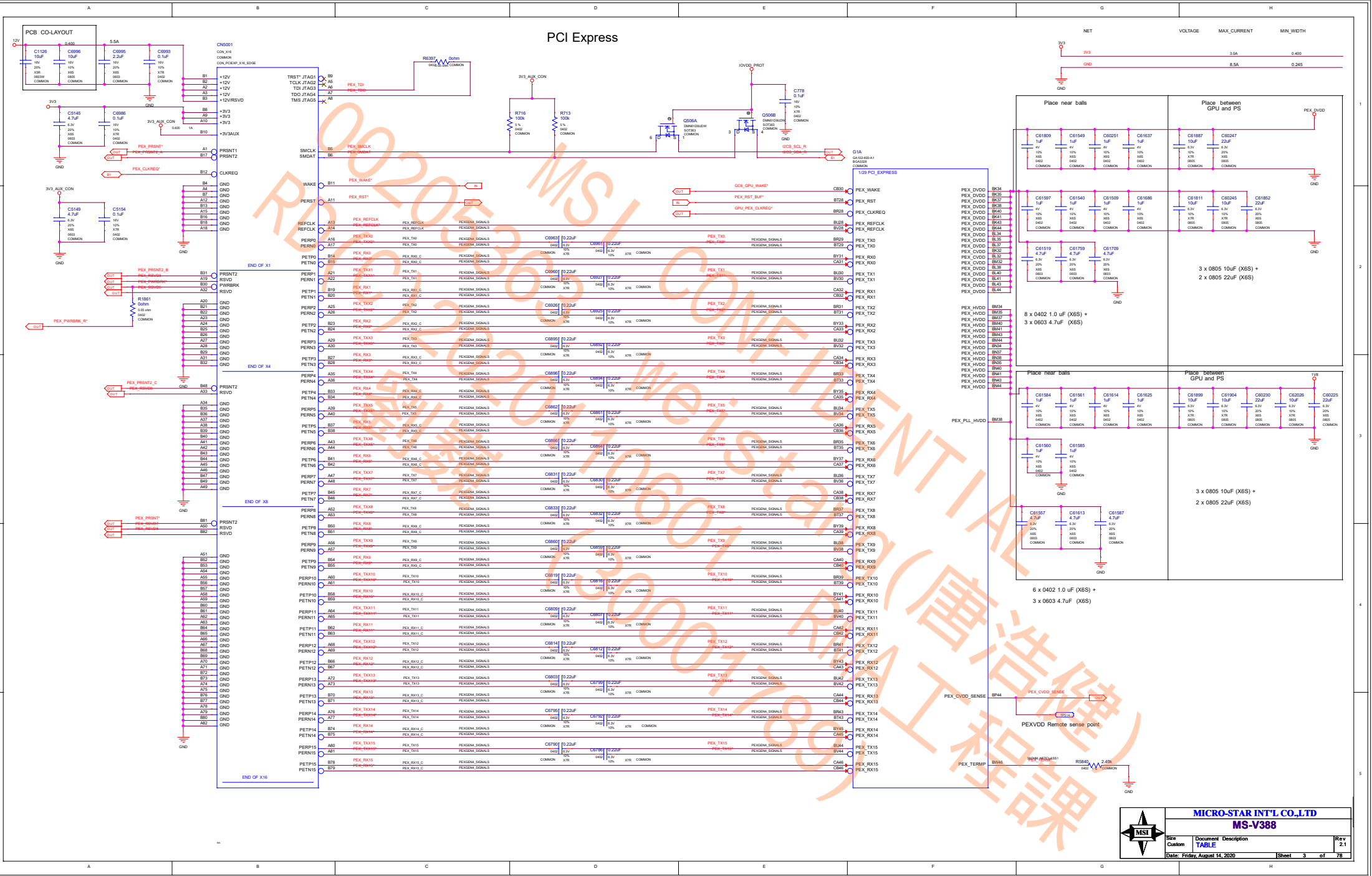
350W, FH Std PCB, 384b, GDDR6X x8  
DP + DP + DP + HDMI/DP

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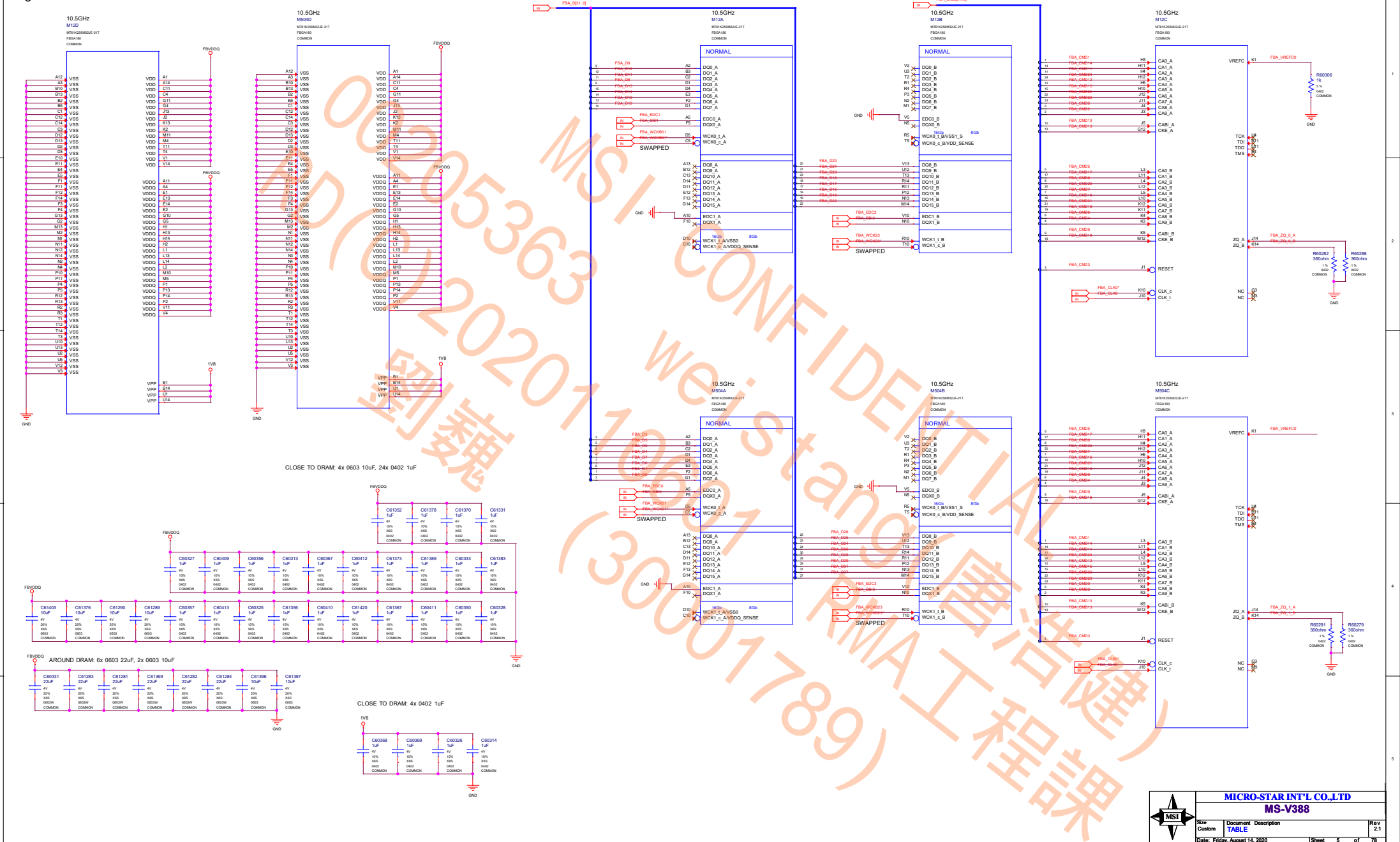
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Block Diagram



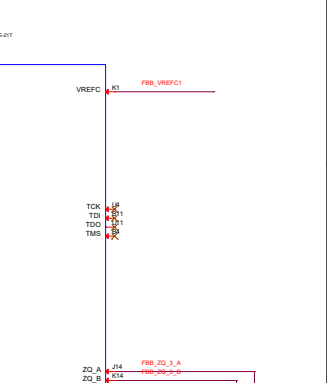




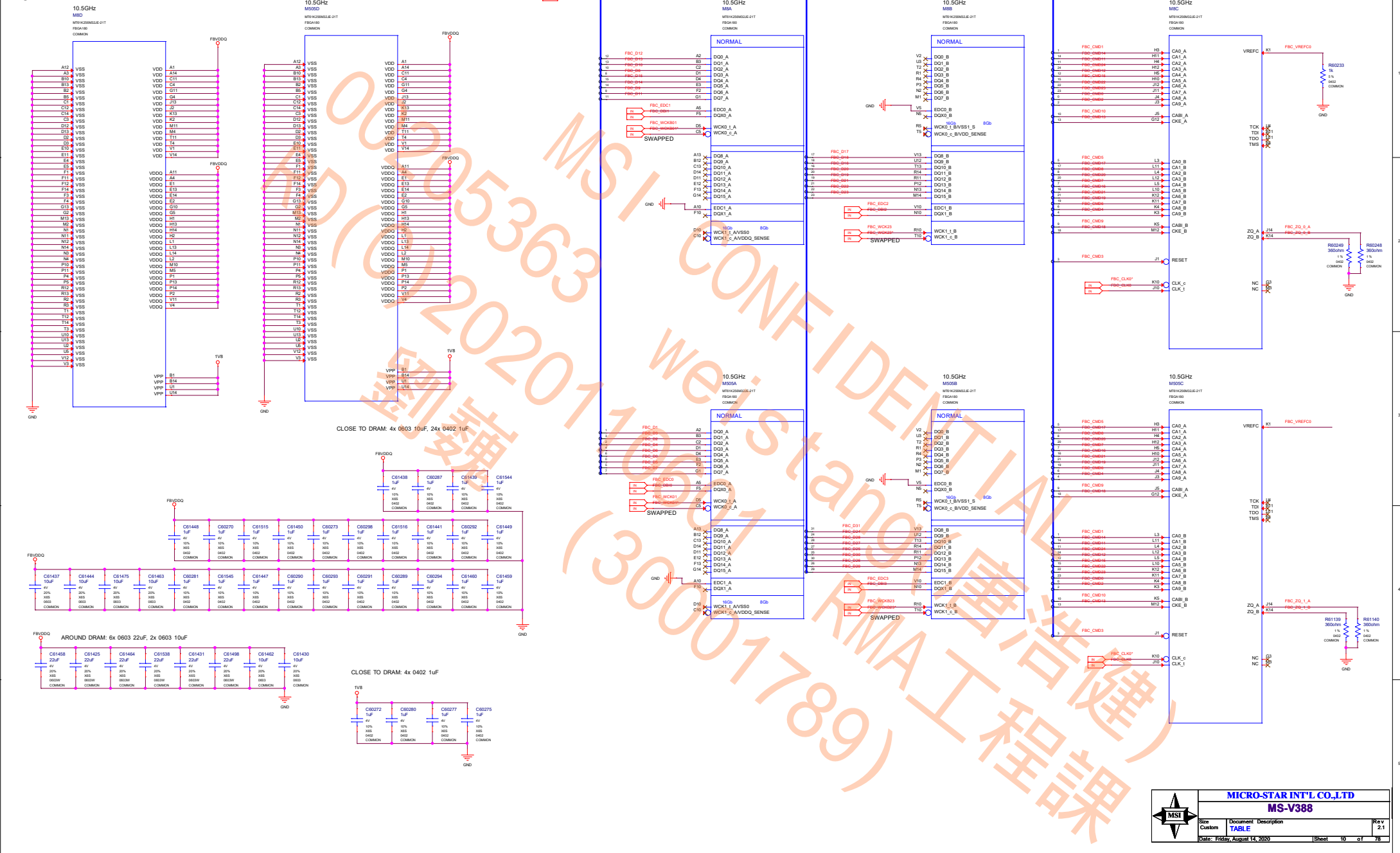












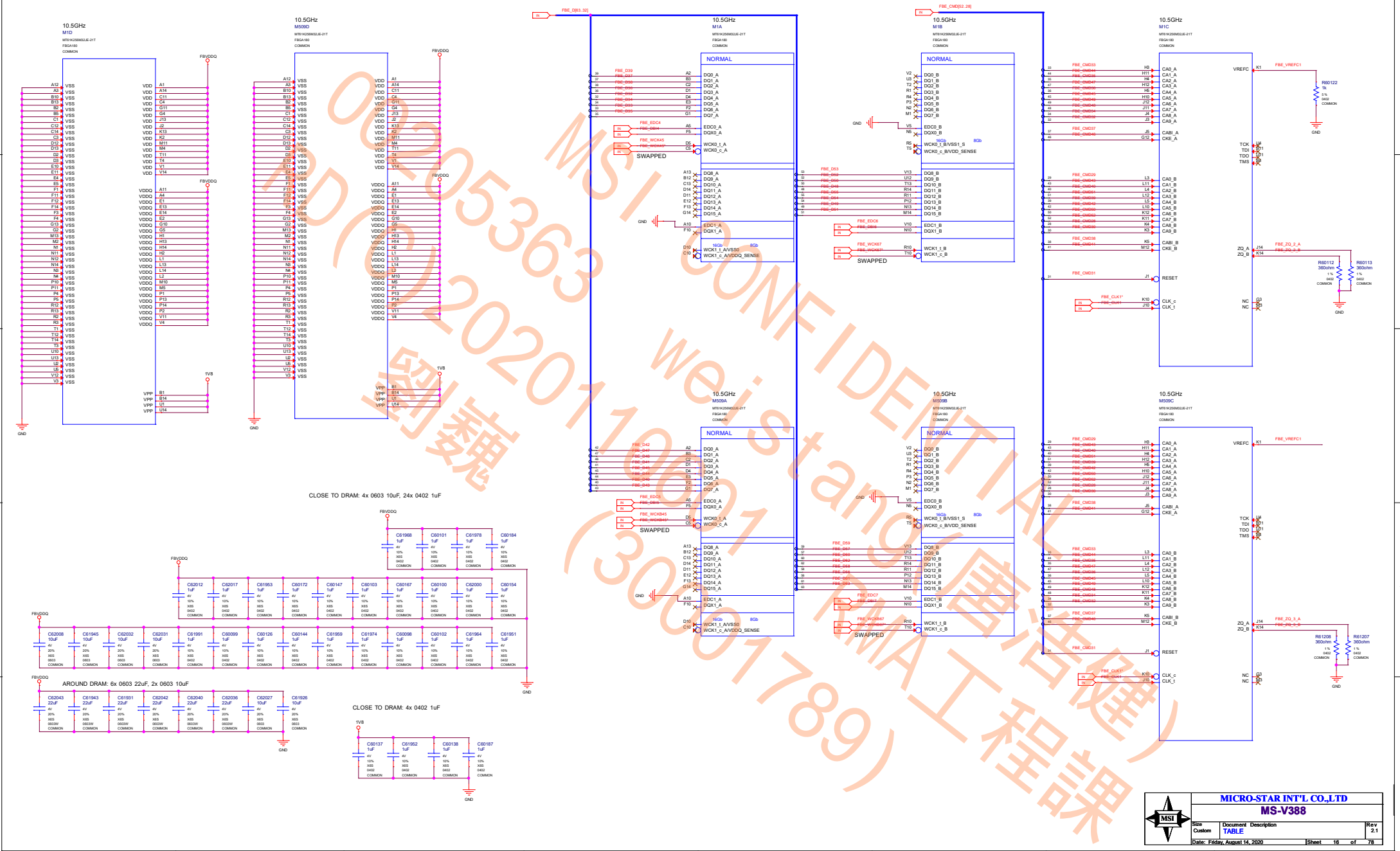






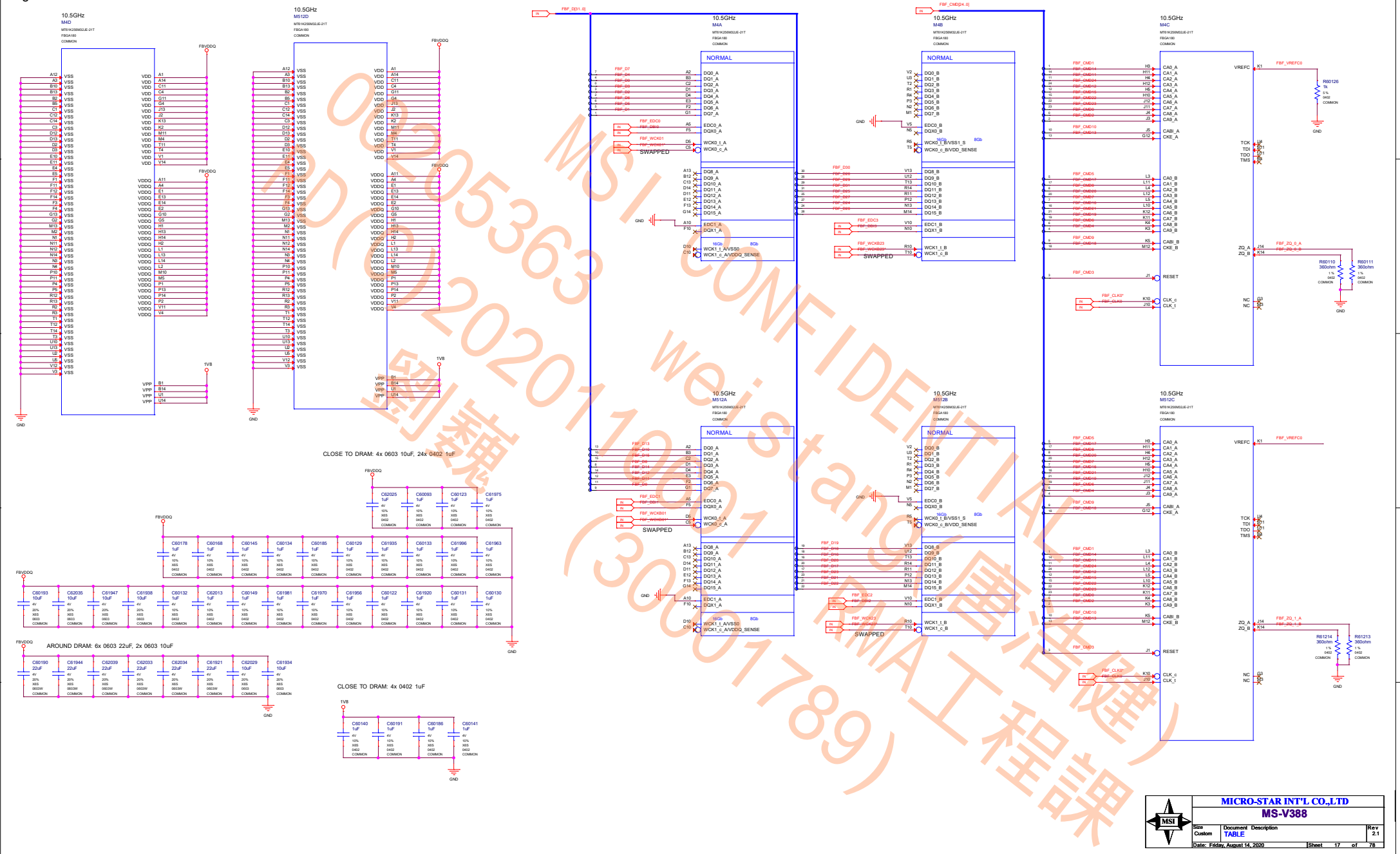


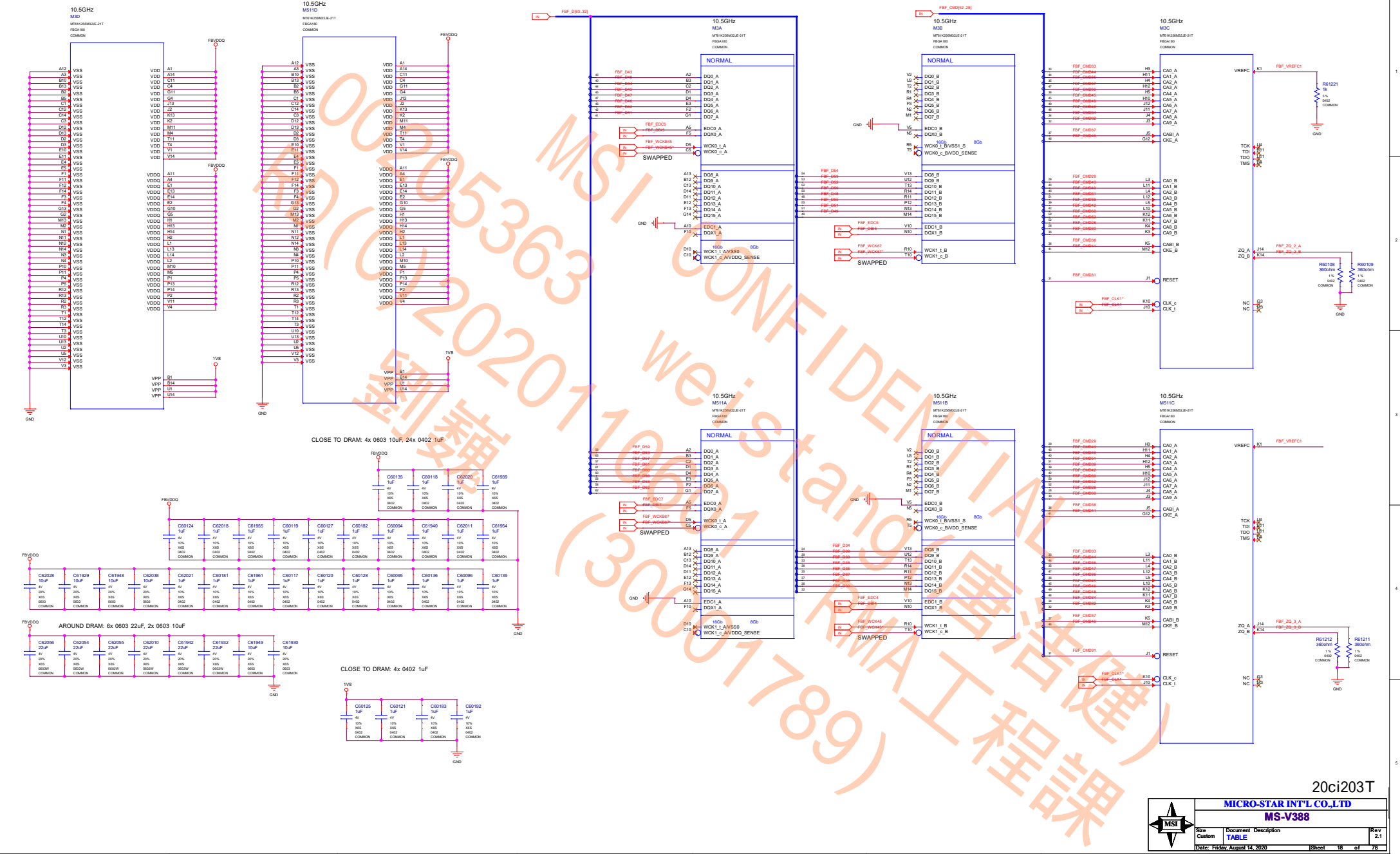




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**MS-V388**

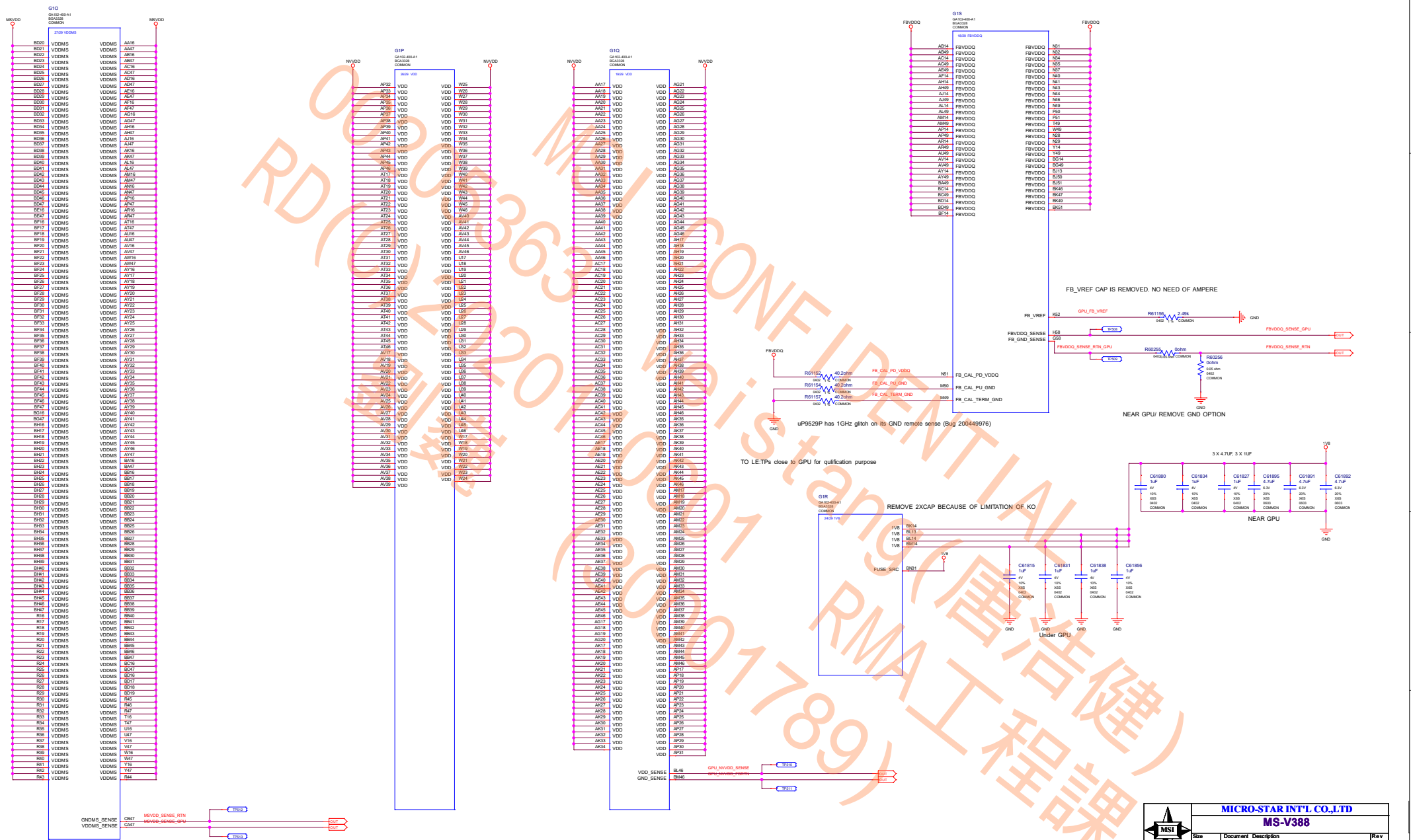
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## GPU PWR and GND

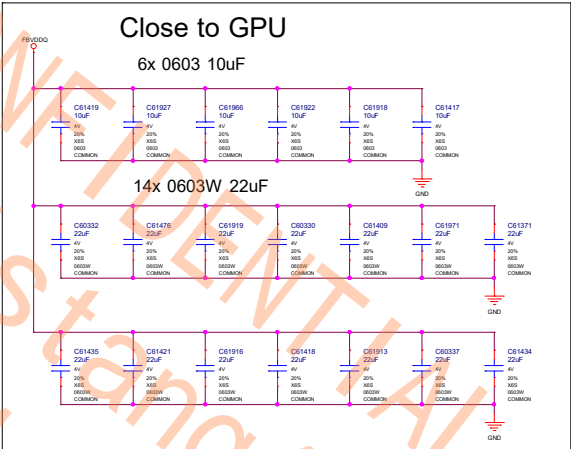


NVVDD

UNDER GPU



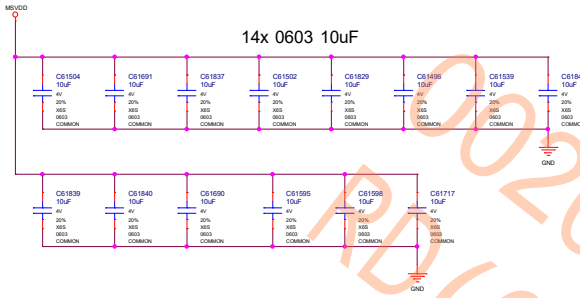
FBVDDQ



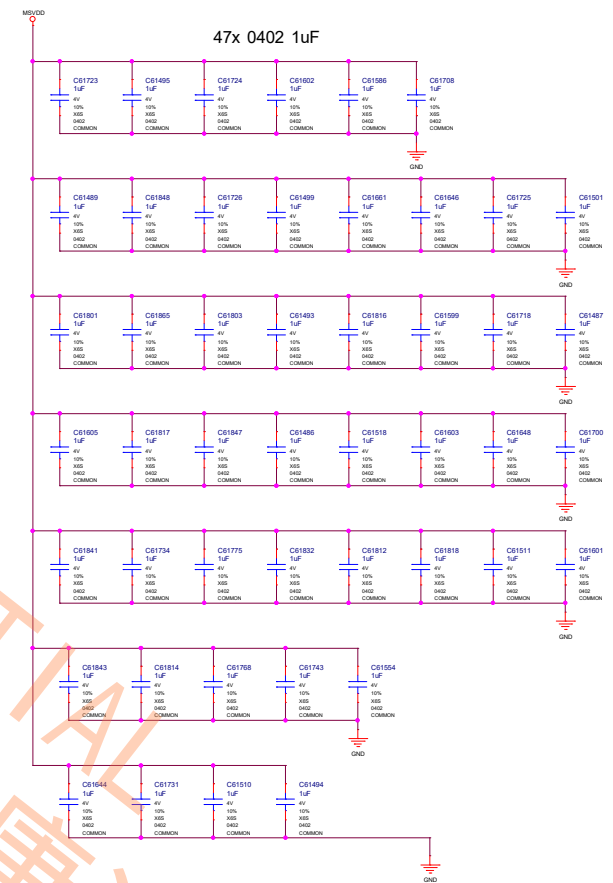
## MSVDD

## UNDER GPU

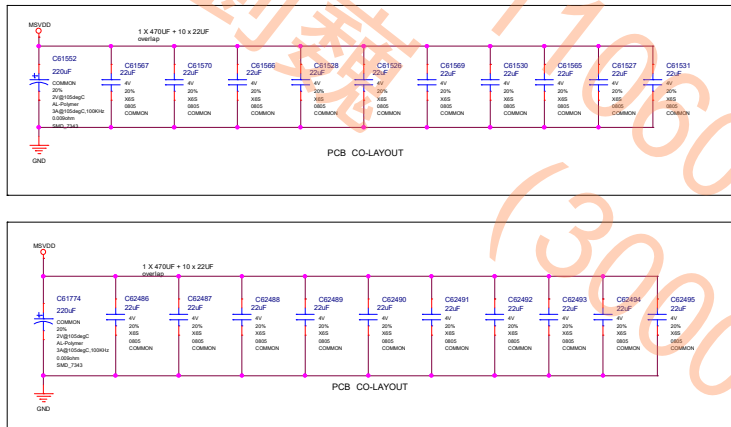
14x 0603 10uF



47x 0402 1uF




2x SMD7343 220uF (EACH CO-LAYOUT WITH 10x 22uF 0805)



REMOVED 3x 1uF 0402 DUE TO SPACE RESTRICTION

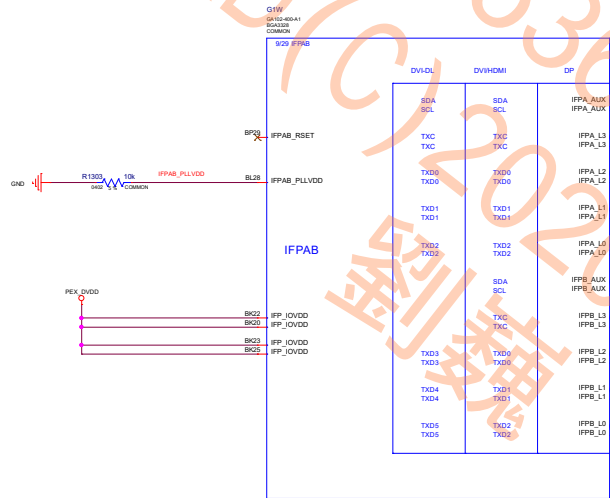
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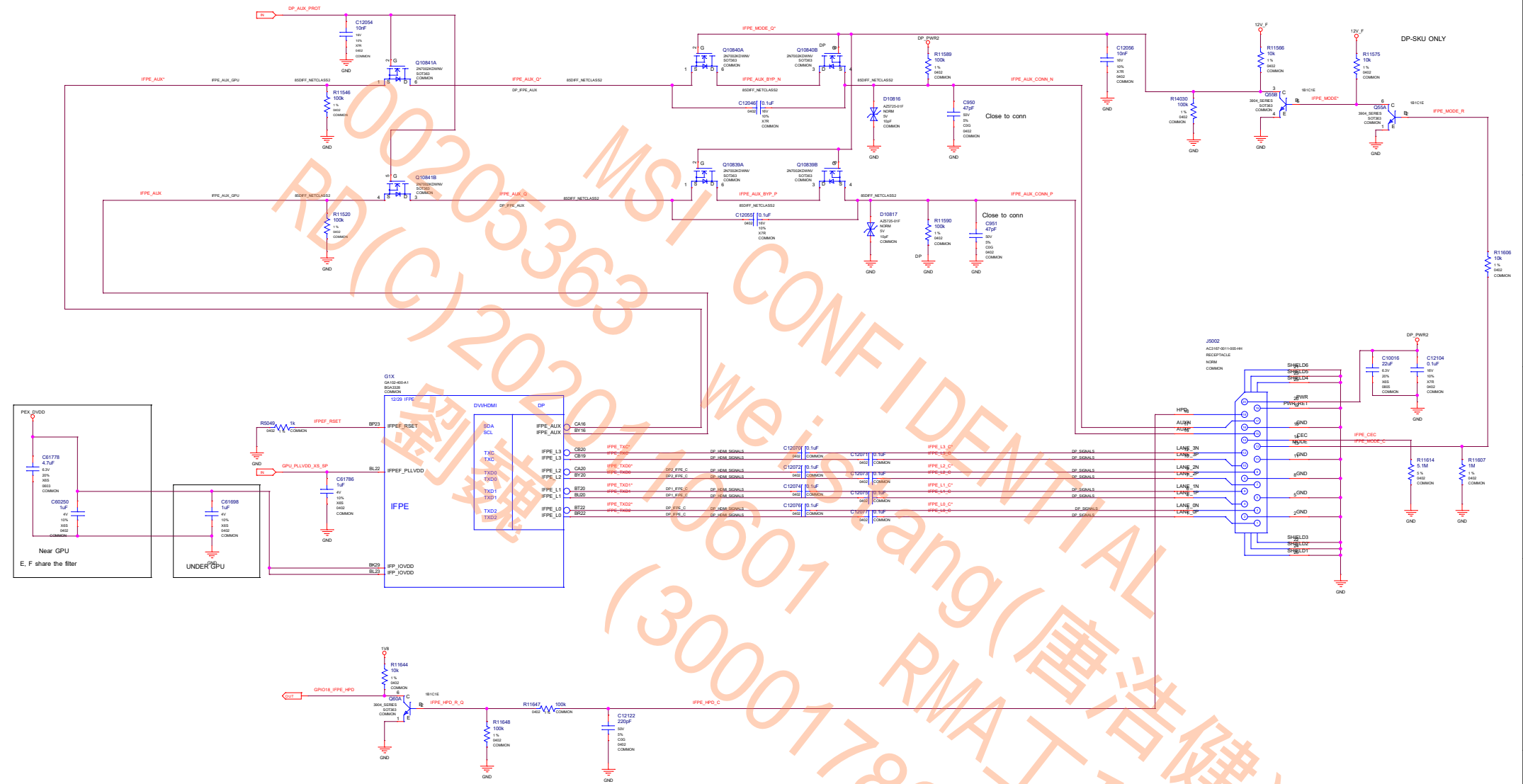
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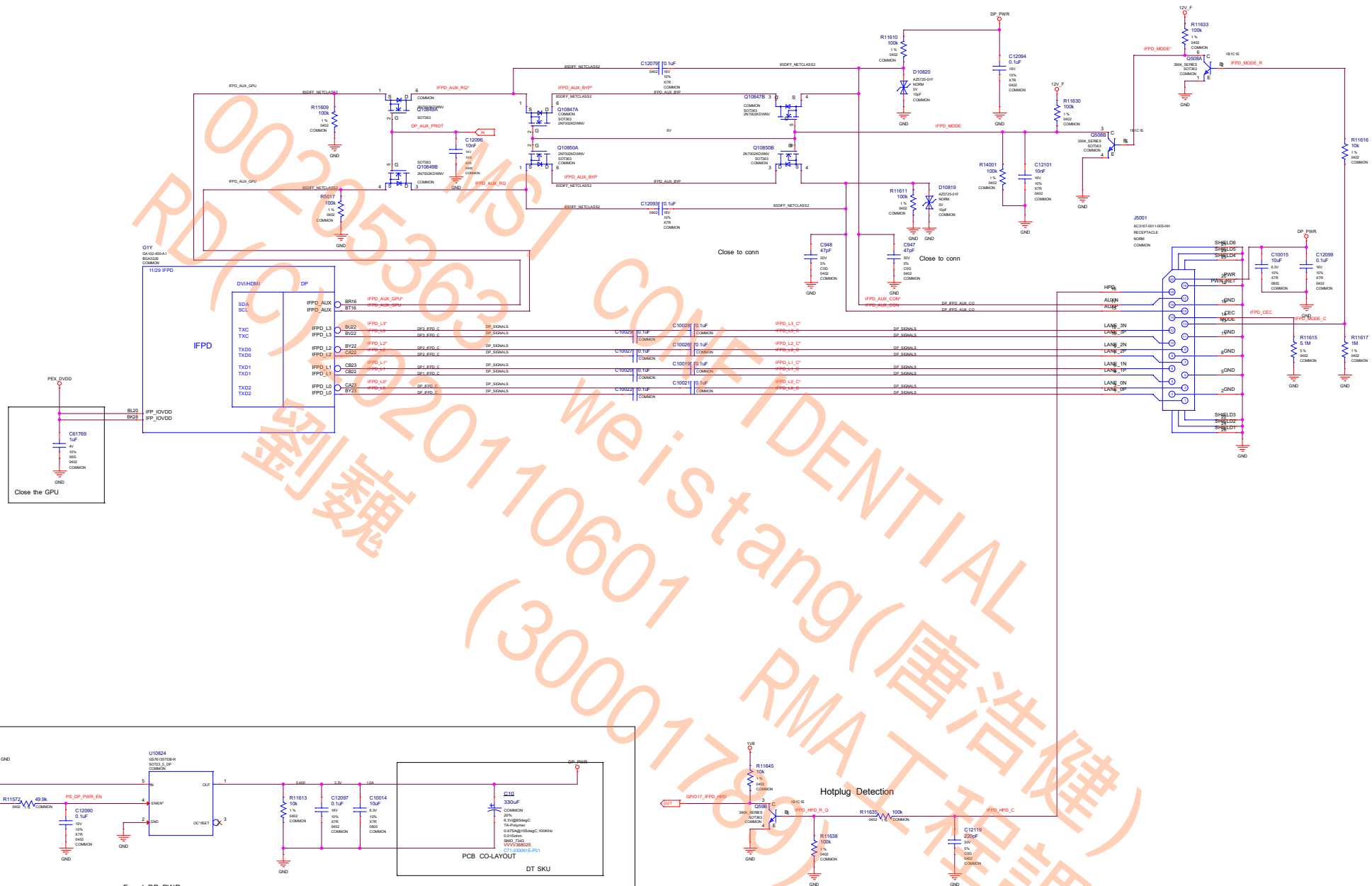
IFPA UNUSED, IFPB UNUSED





20ci203T

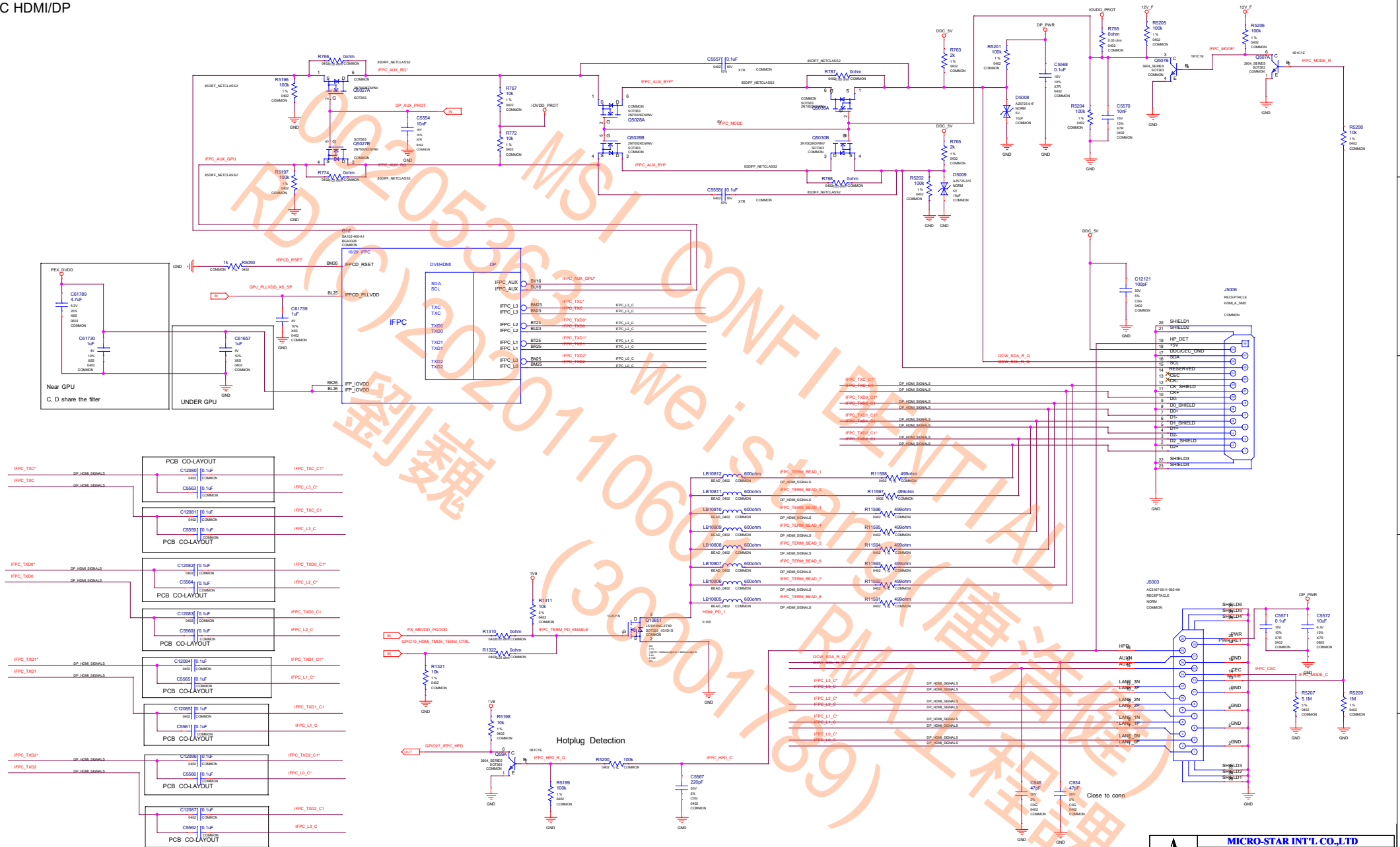
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Fused DP\_PWR

Hotplug Detection

## IFPC HDMI/DP



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MISC: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG MICRON 8Gb 19Gbps
L	H	L	00010	RAMCFG TBD
H	L	L	00100	RAMCFG TBD
H	L	H	00101	RAMCFG TBD
H	L	H	00101	RAMCFG MICRON 8Gb 21Gbps

DEFAULT

H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

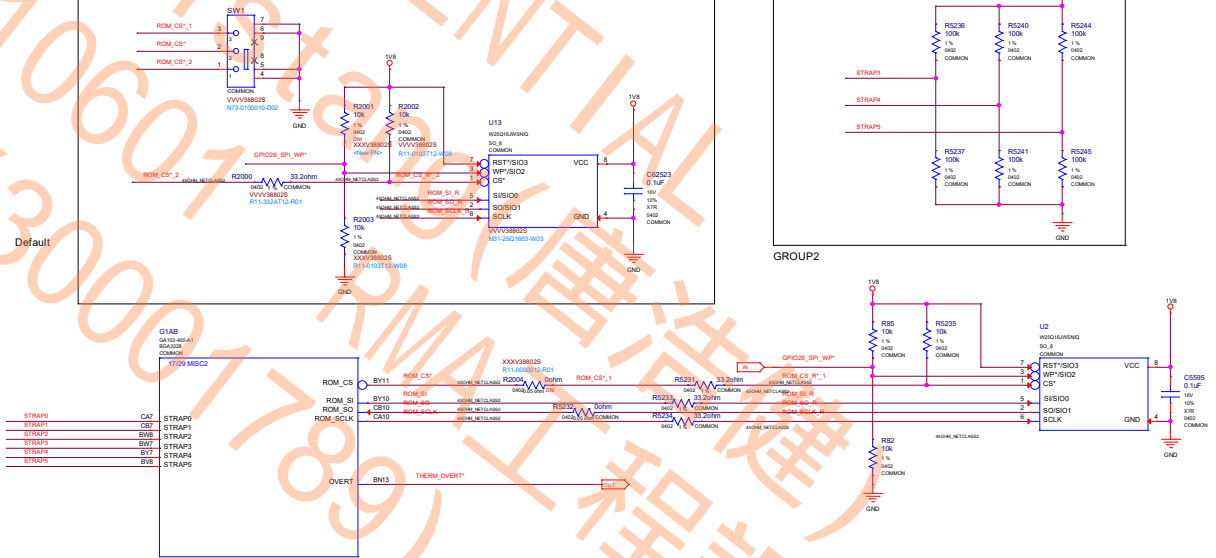
ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0],FS_OVERT	1:ENABLE 0:DISABLE
H	H	H	0111	FS_OVERT ENABLE
L	L	L	0000	FS_OVERT DISABLE

DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	H	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	0	1
H	L	H	0	1	0	0
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

Default

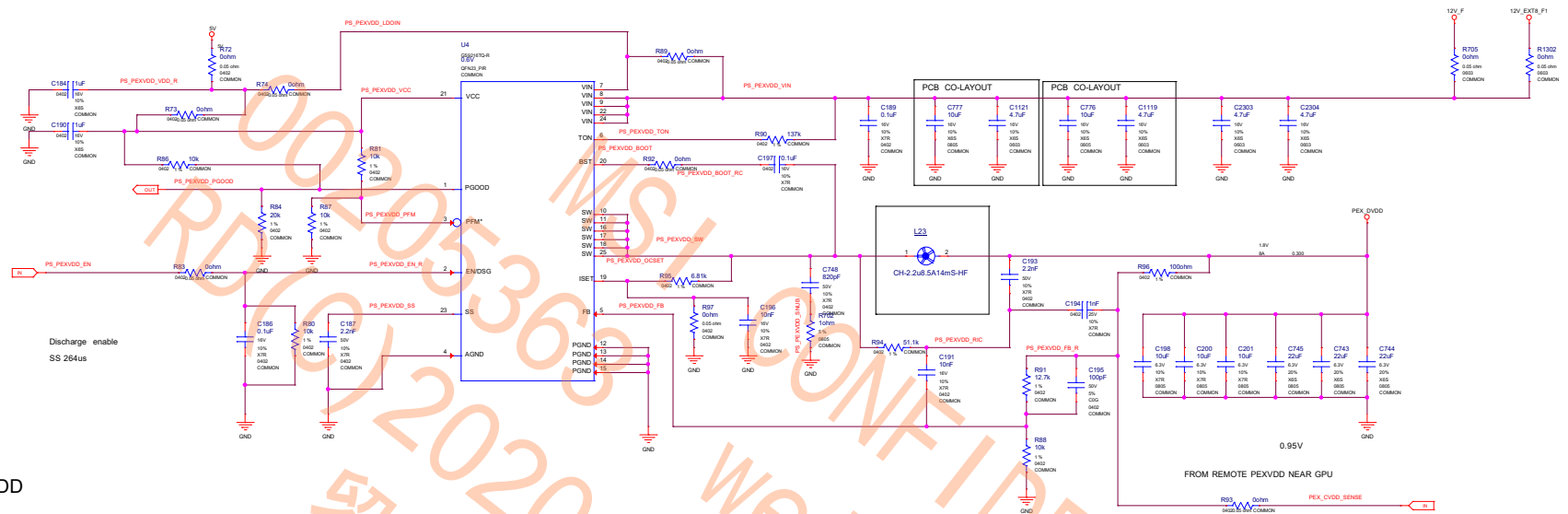
Dual BIOS



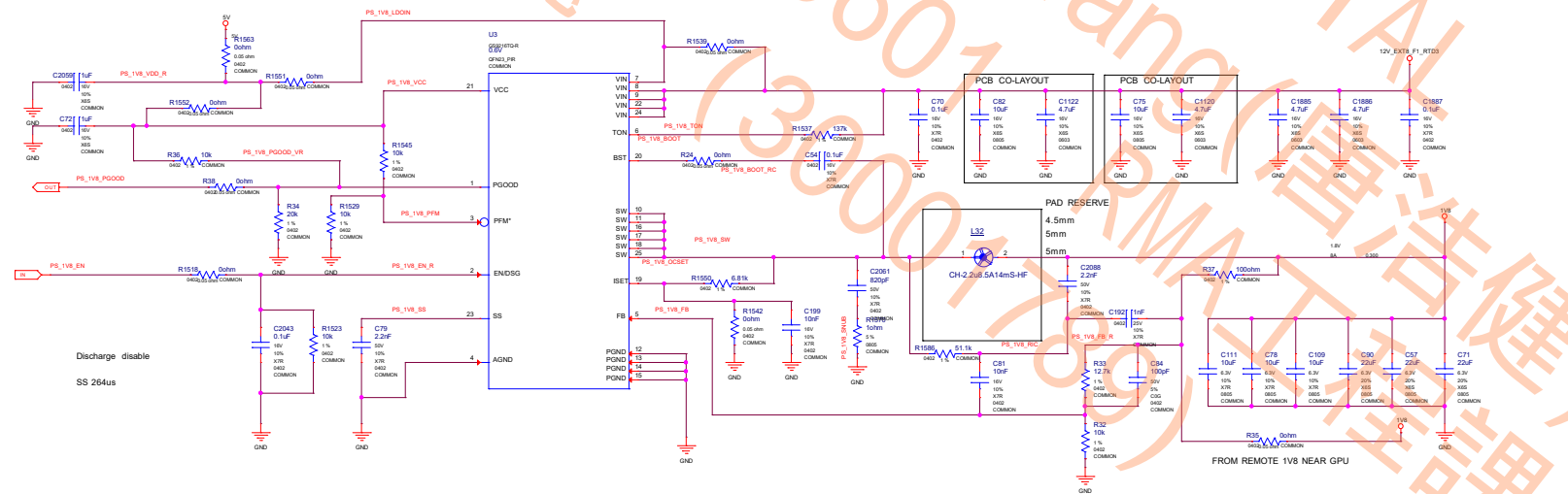




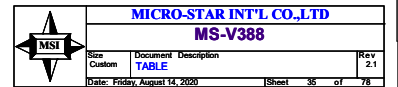
## PS: PEX\_DVDD 1V8 Rail




PEX\_DVDD



1V8



BLANK

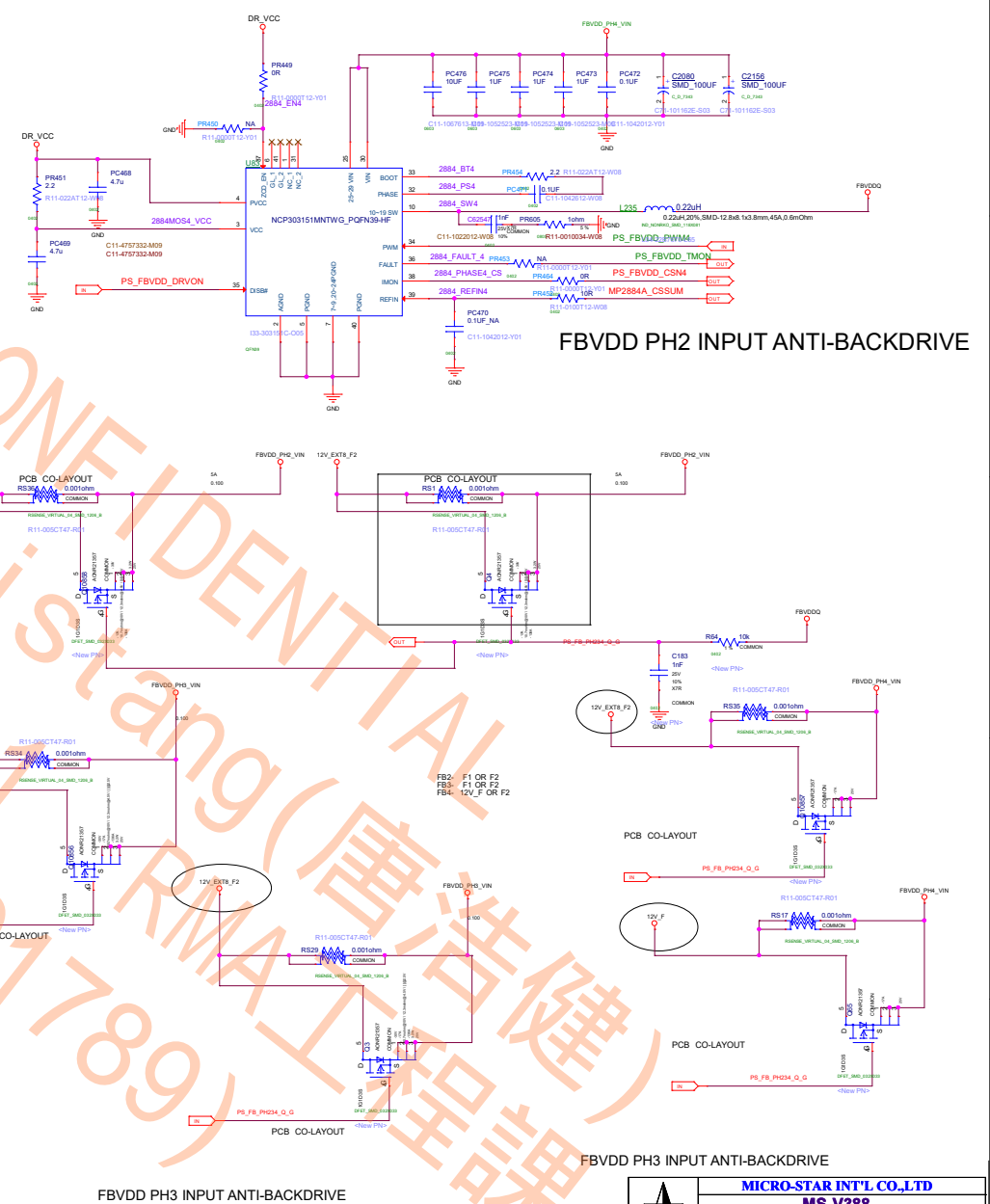
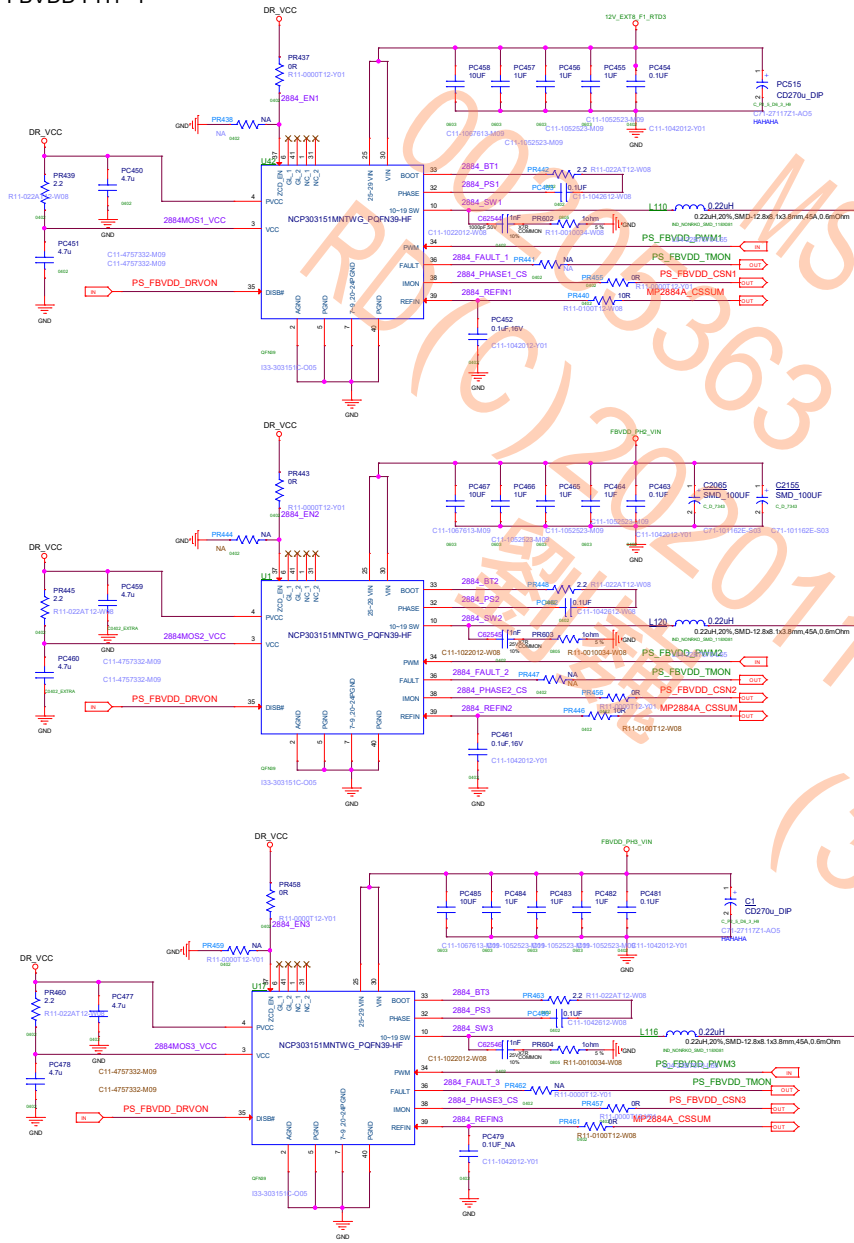
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# PS: FBVDD PH1~4




## FBVDD PH2 INPUT ANTI-BACKDRIVE

## FBVDD PH3 INPUT ANTI-BACKDRIVE

## FBVDD PH3 INPUT ANTI-BACKDRIVE

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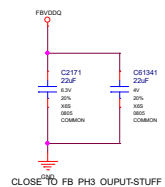
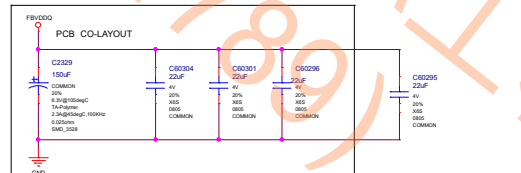
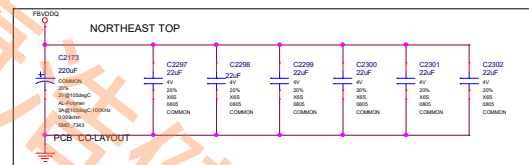
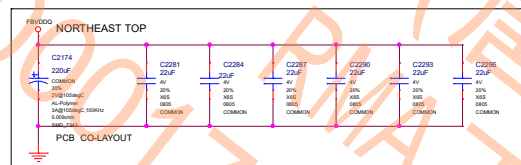
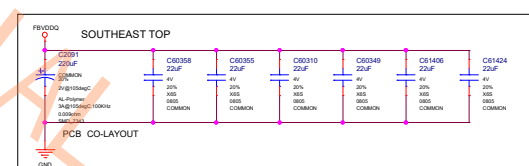
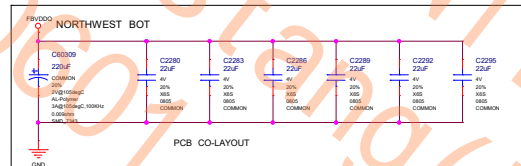
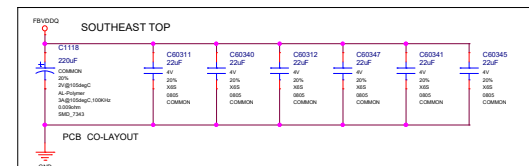
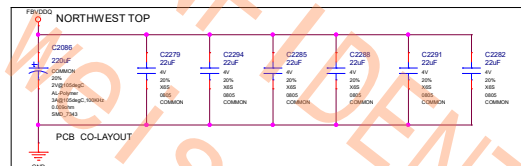
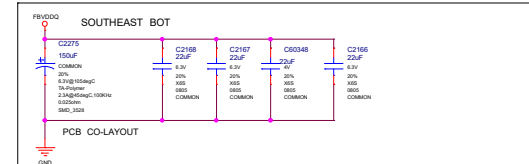
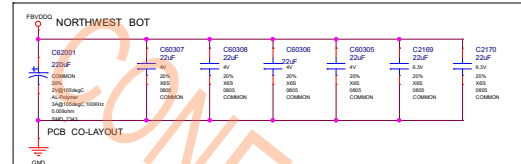
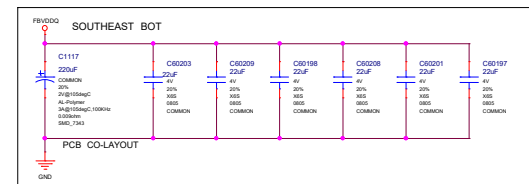
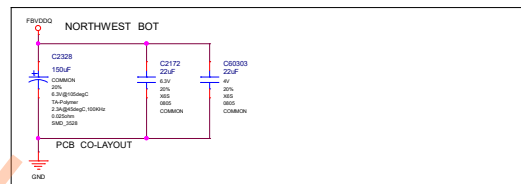
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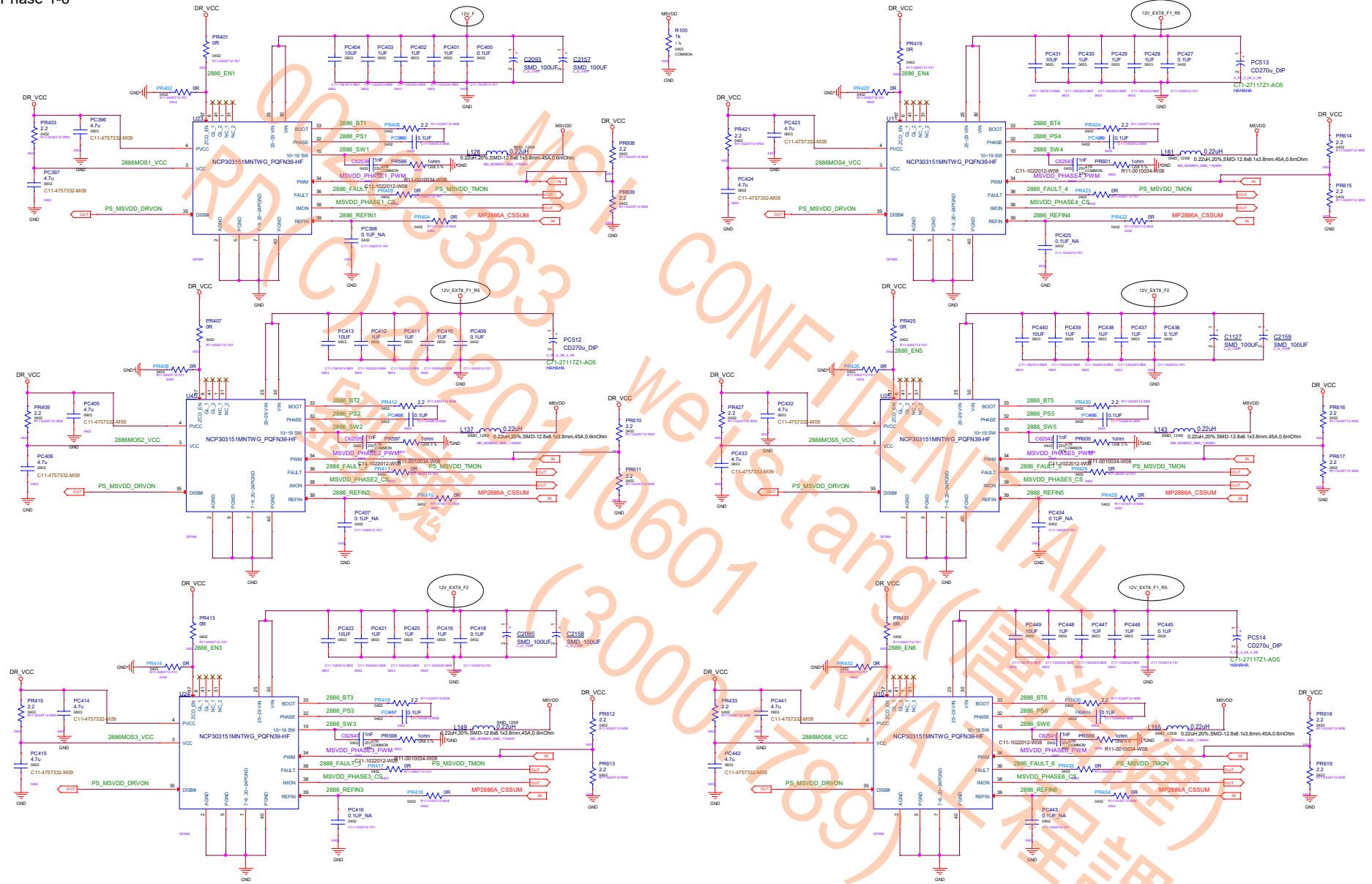
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REFER TO PCB FOR BOM STUFFING






## MSVDD Phase 1-6



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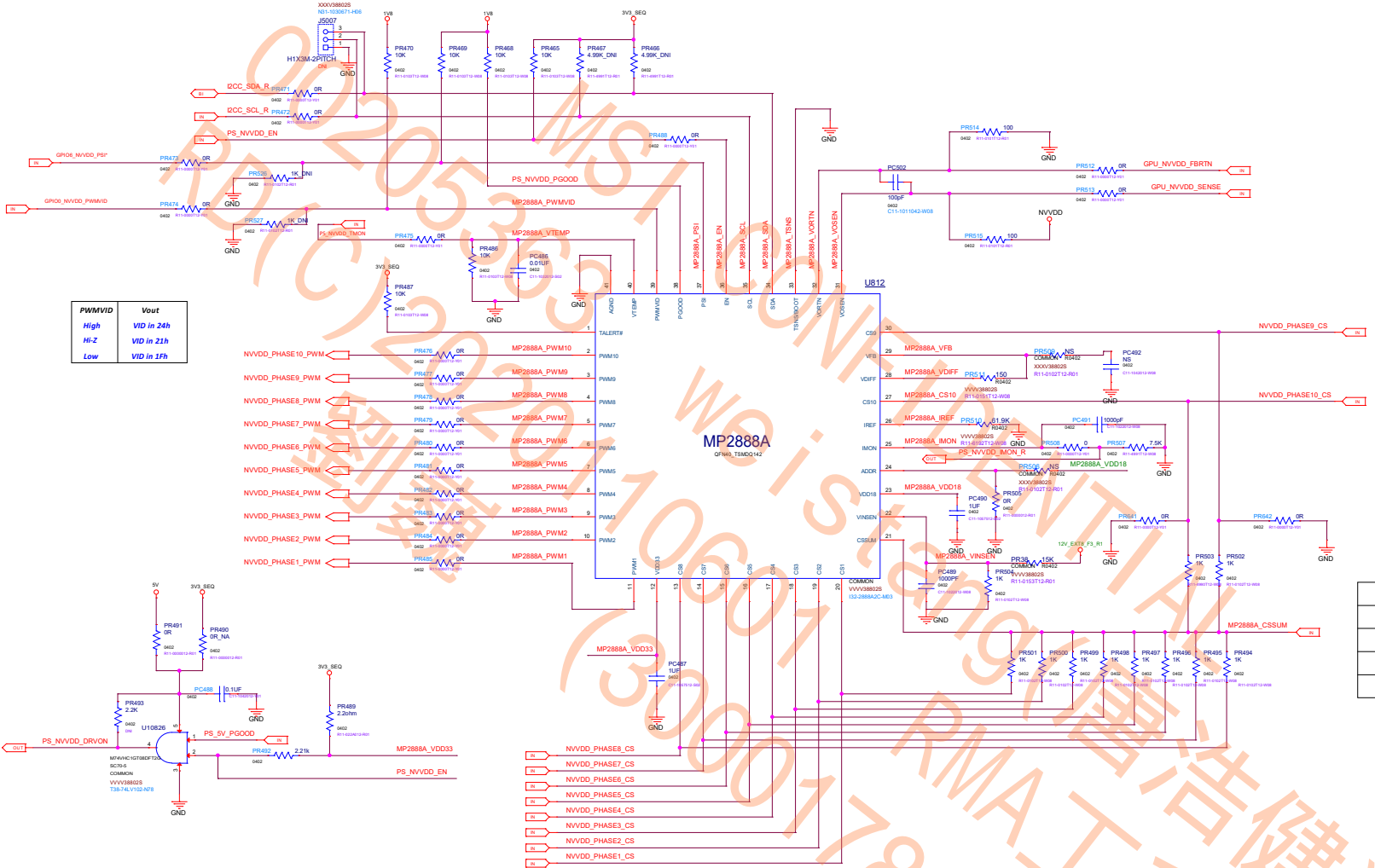
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PWMVID	Vout
High	VID in 24h
Hi-Z	VID in 21h
Low	VID in 1fh

EN Type	R3
Open Drain	10k
Push Pull	N5

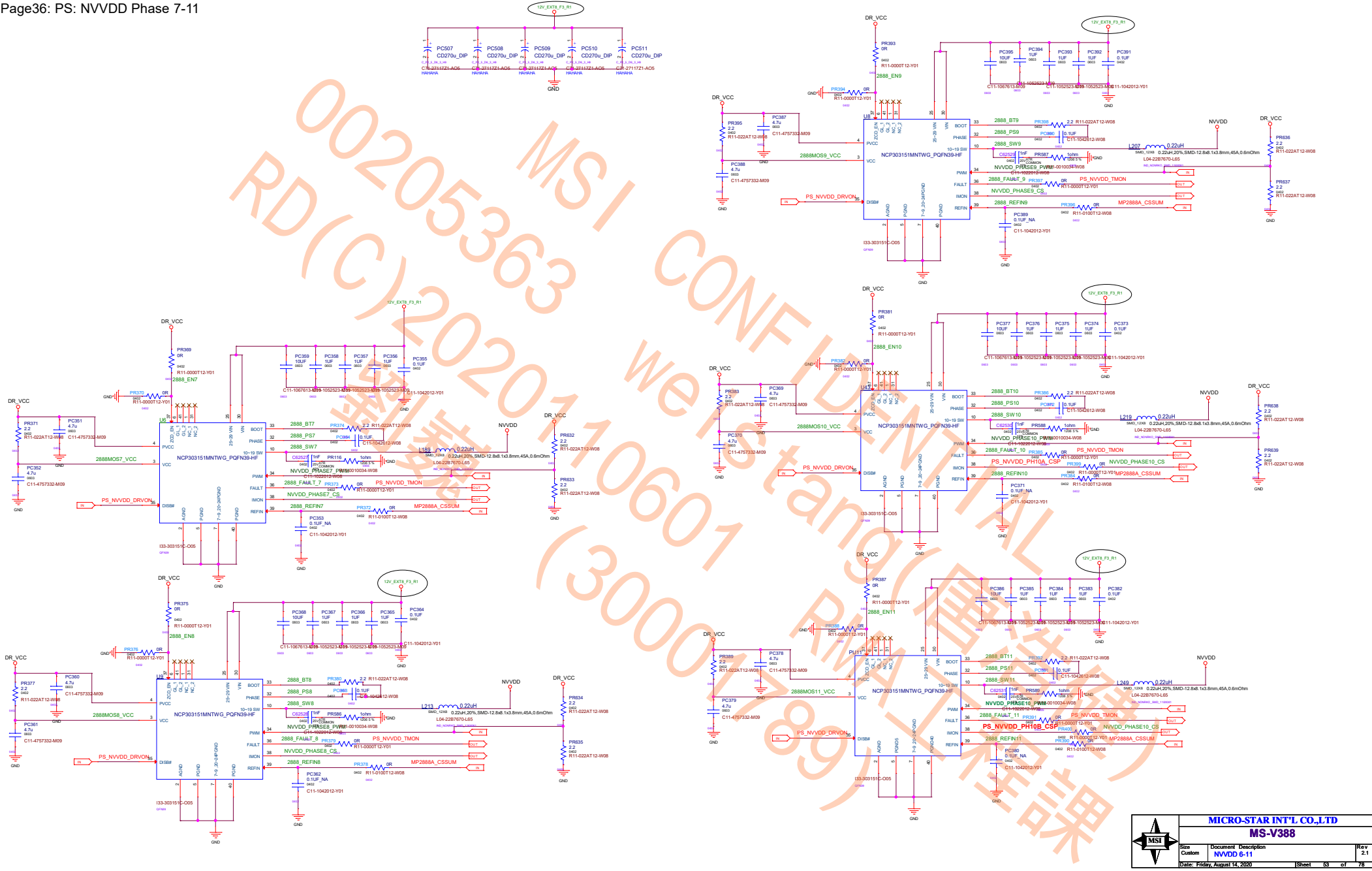
  

PS1	Mode
High	High Phase Count
Hi-Z	Auto Power Mode
Low	Low Phase Count

PMBus Address	Setting Point(V)	R <sub>load</sub> (kΩ) 1%	R <sub>load</sub> (kΩ) 1%
20h	0	-	0
21h	0.031	3.32	0.059
22h	0.057	3.32	0.111
23h	0.084	3.32	0.162
24h	0.116	3.32	0.226
25h	0.156	3.32	0.316
26h	0.205	3.32	0.43
27h	0.266	3.32	0.576
28h	0.340	3.32	0.768
29h	0.430	3.32	1.05
2Ah	0.540	3.32	1.43
2Bh	0.675	3.32	2
2Ch	0.844	3.32	2.94
2Dh	1.048	3.32	4.64
2Eh	1.301	3.32	8.66
2Fh	1.500	3.32	16.5

	+NVVDD
TDC	200A
IccMax	330A
Vboot	0.8V
Load Line	0mohm






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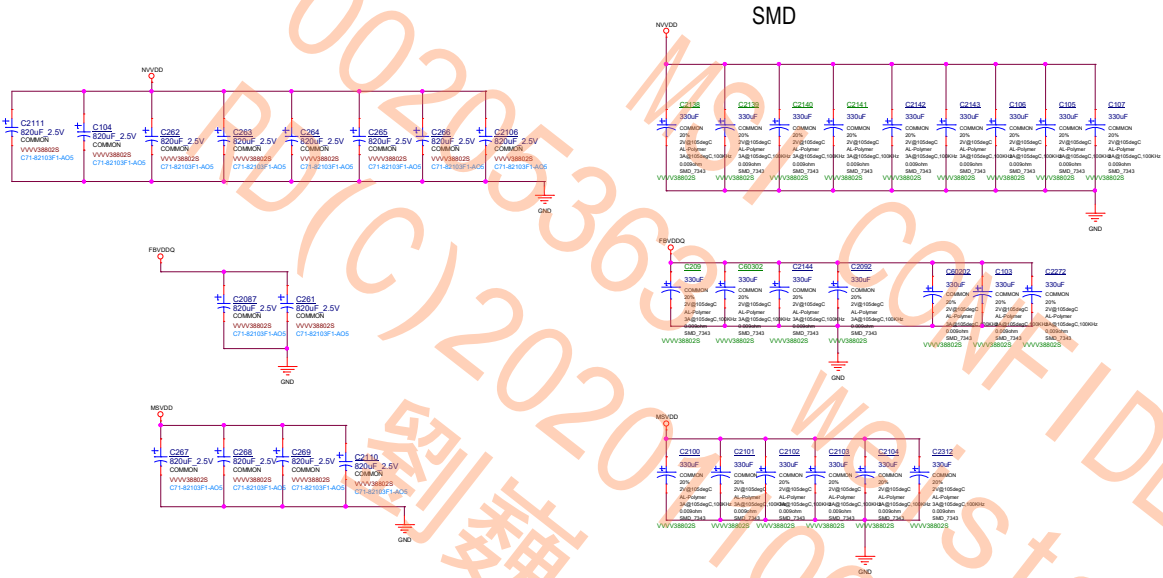
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PS: NVVDD OUTPUT CAP(TOP)



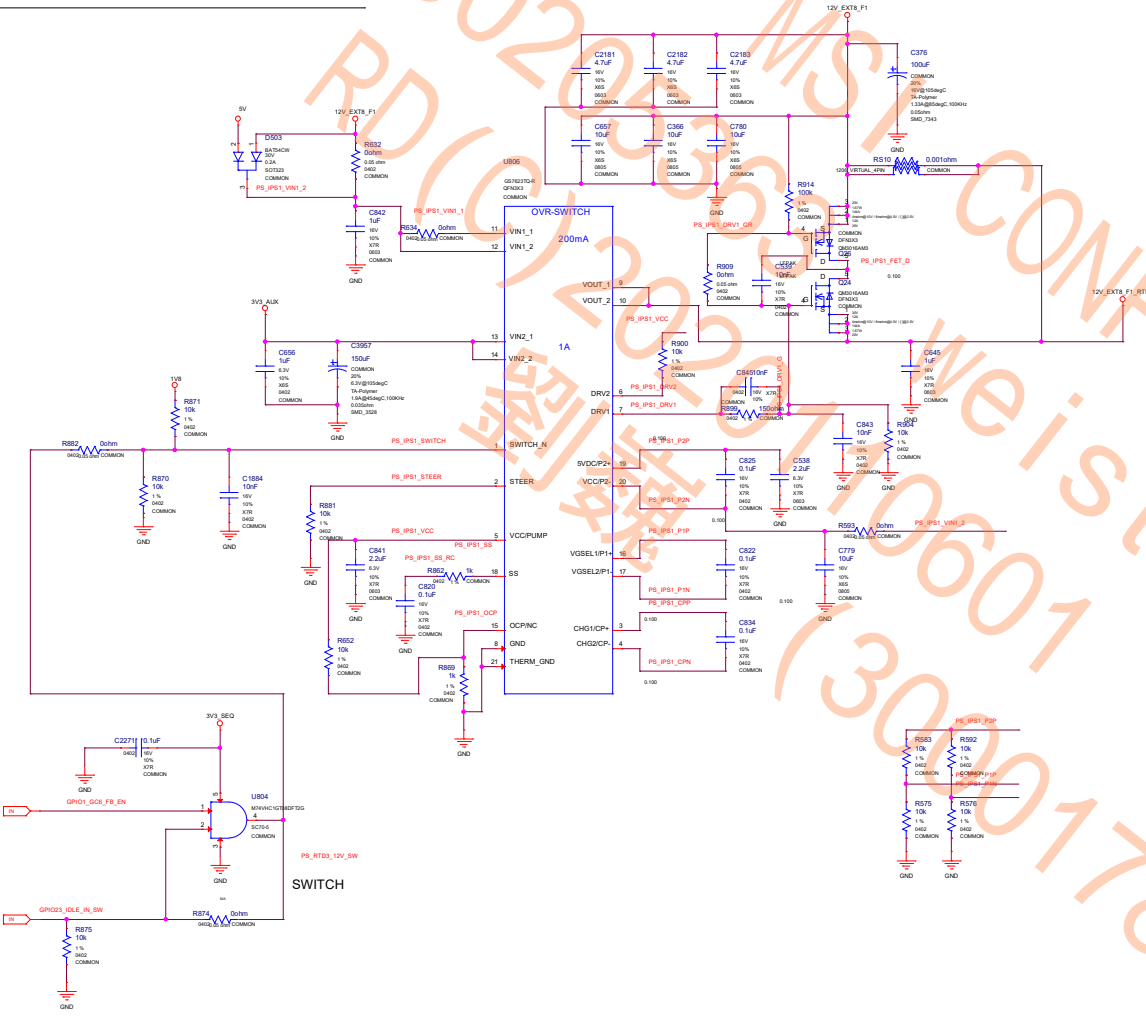
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PS: INPUT SWITCH RTD3

AND GATE LOGIC FOR P-BOARD

GPI01	GPI023	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A



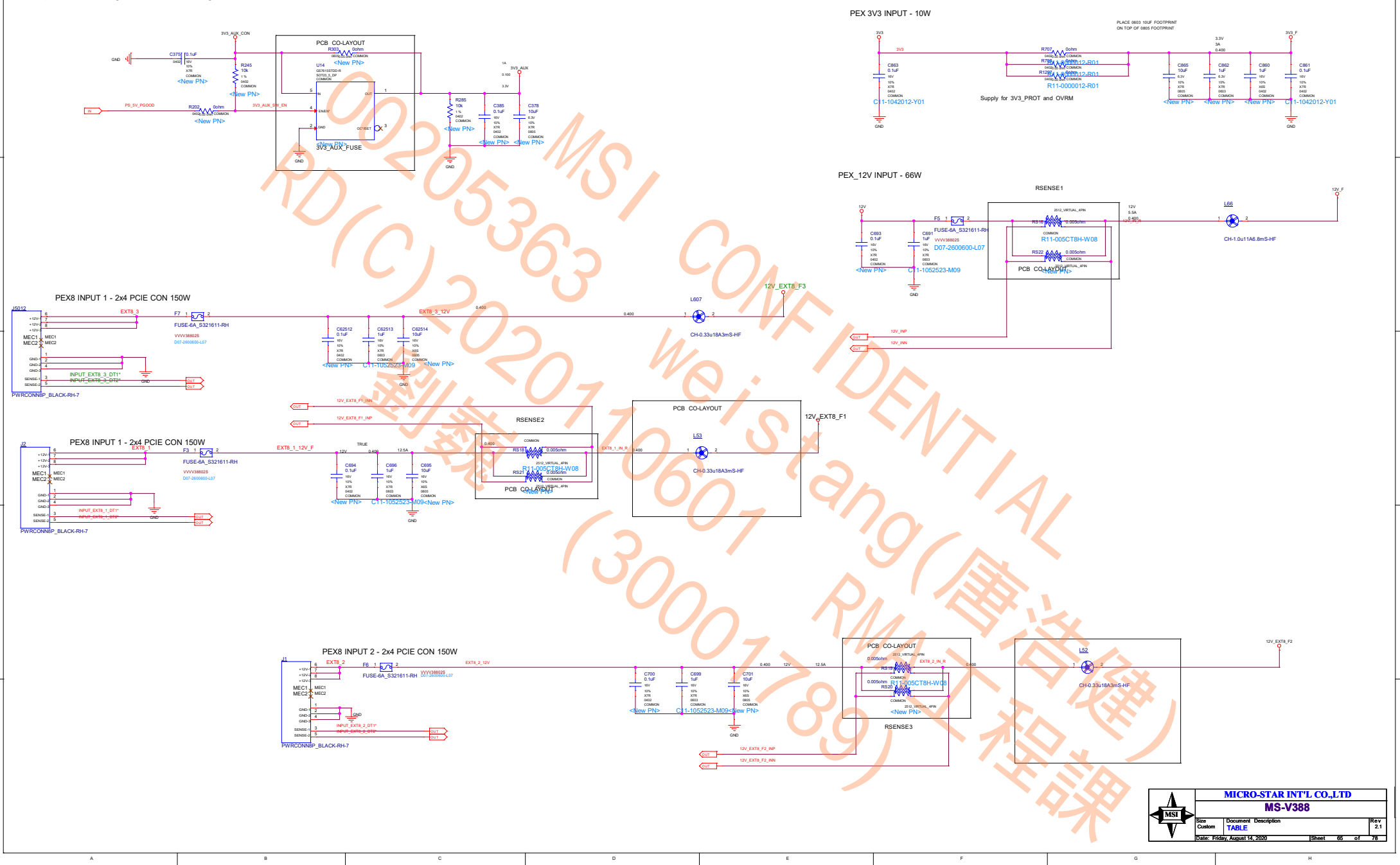
LED\_A

LED\_B

LED\_C

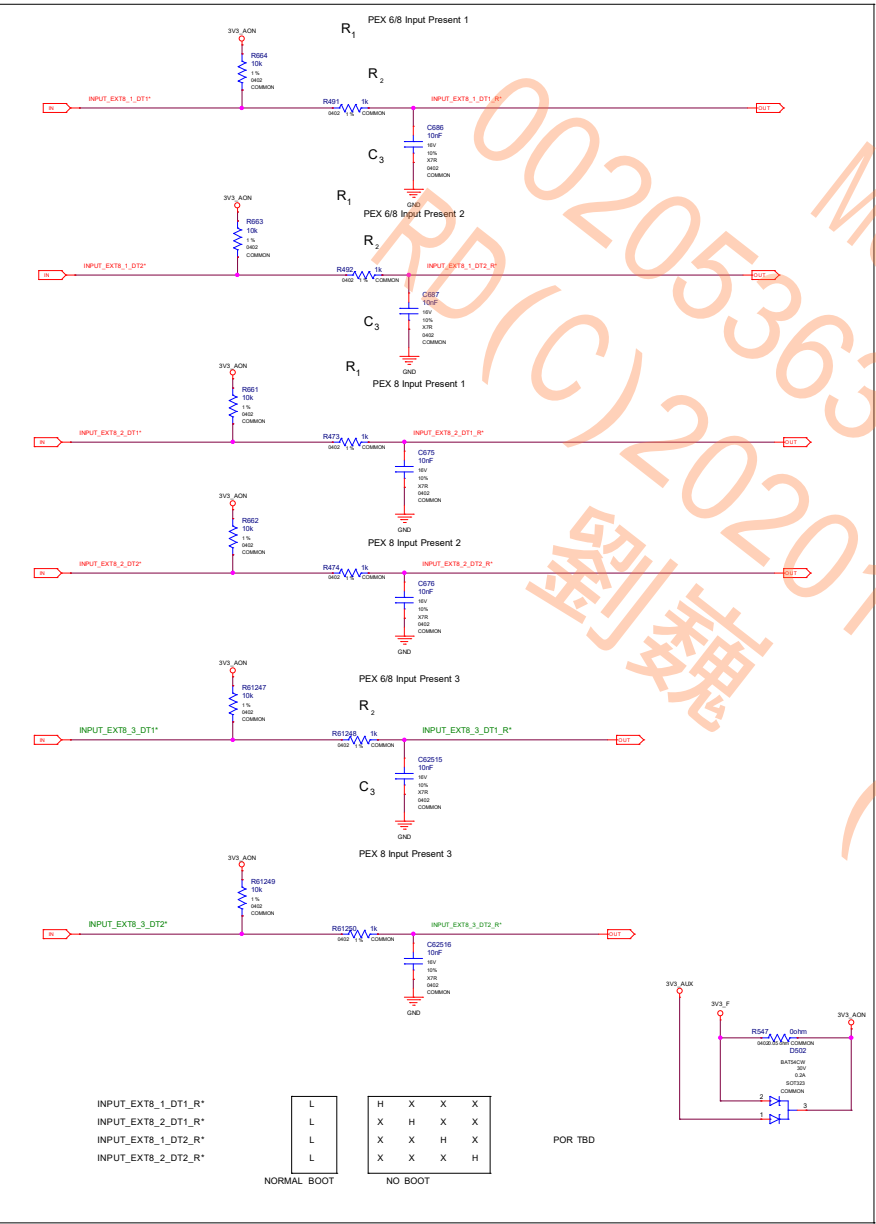
LED\_D

# PS: Inputs, Filtering, and Monitoring



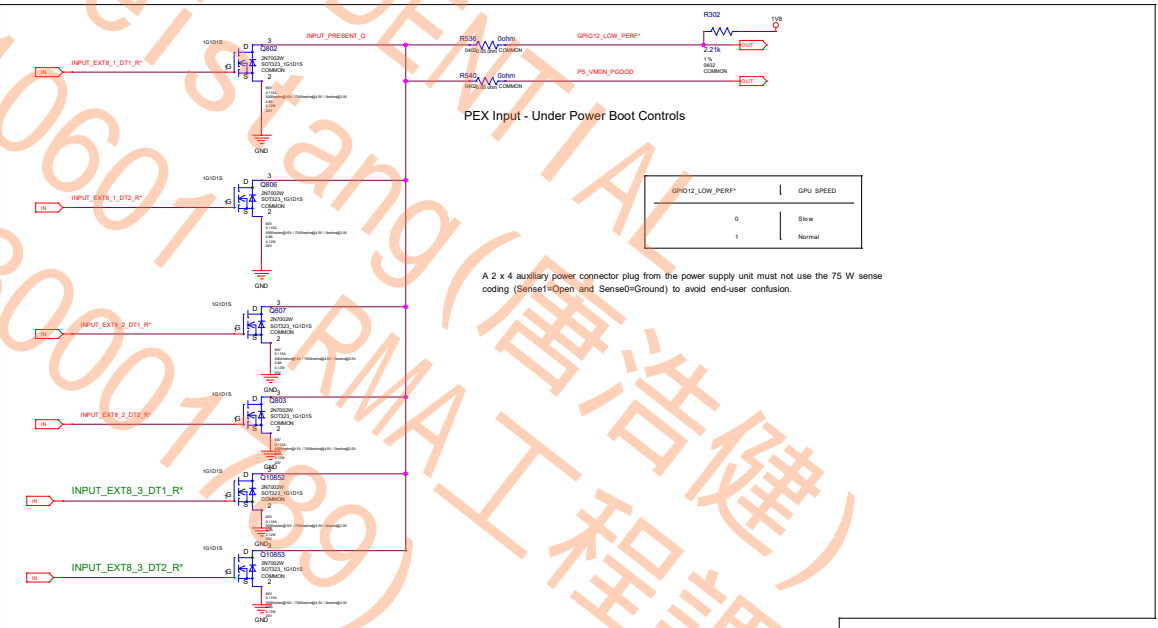
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PS: 12V Current Steering & Hot Unplug Detect



The "Hot Unplug" circuit is optional.

REMOVE HOT UNPLUG



PS: Discrete Steering

Power Supply Features

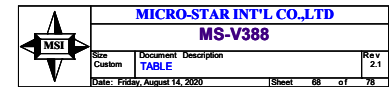
► "Low Performance Boot" feature is optional.

REMOVE steerin

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## Route the trace to PEX Golden Finger

STUFF IF USING 2XMUX

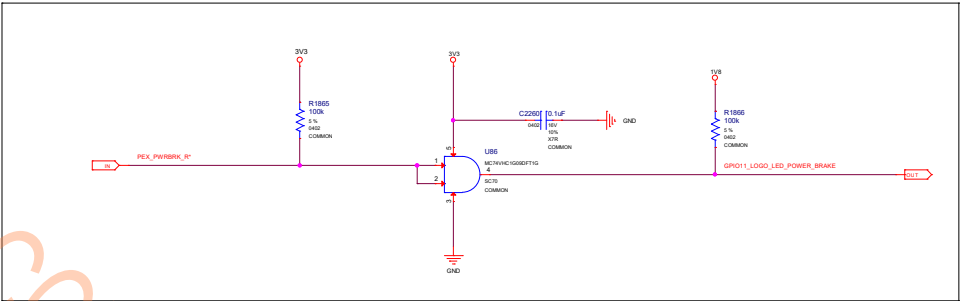
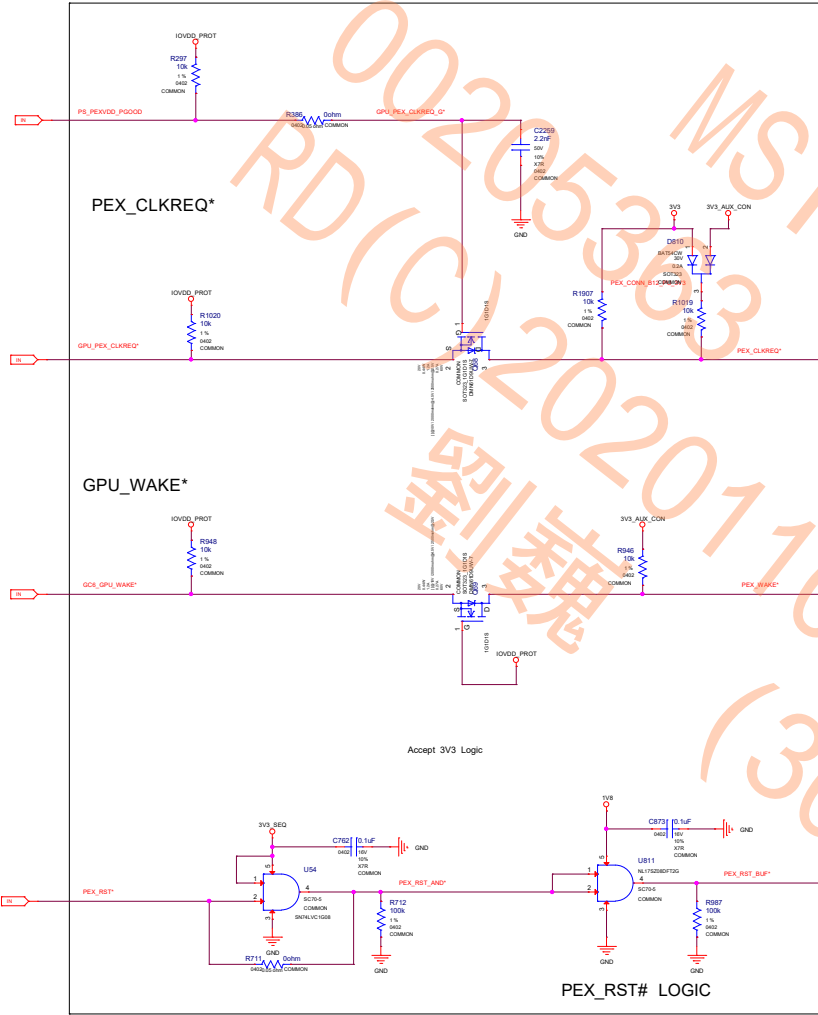






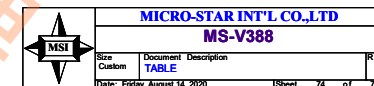
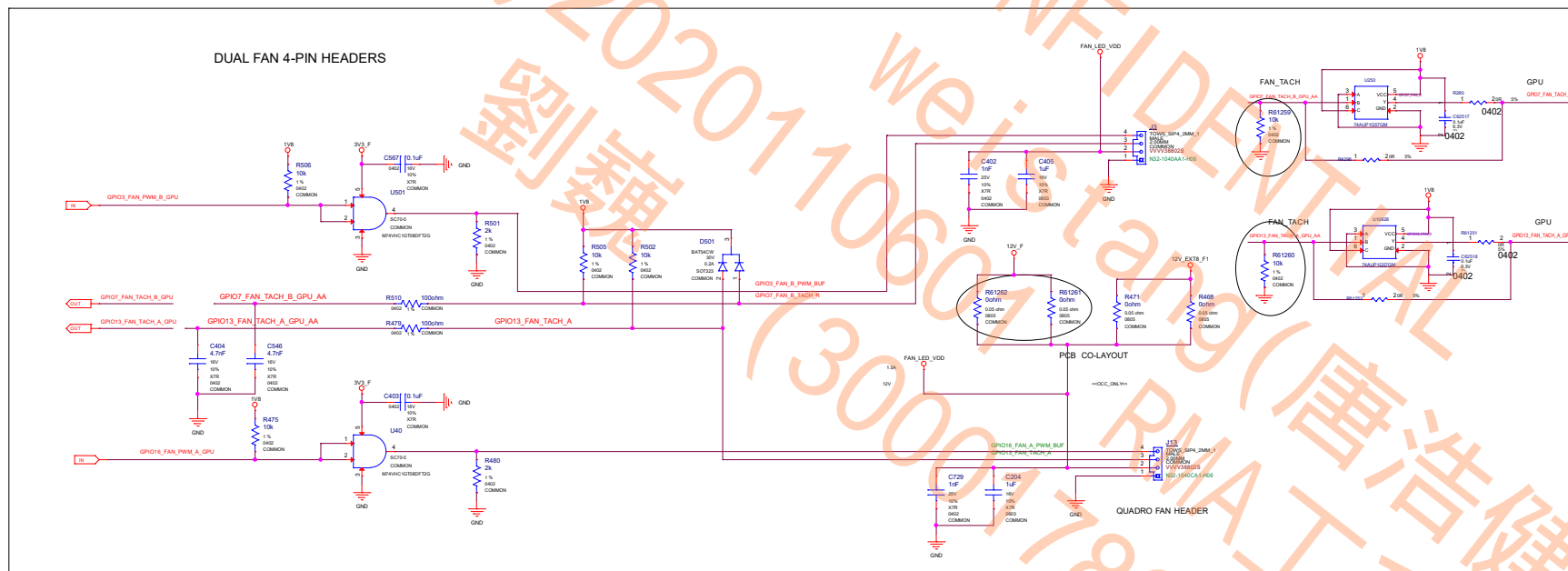







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```
remove LED /GPIO 35
```

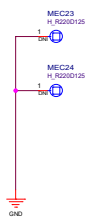


MISC: RGBW LED REF

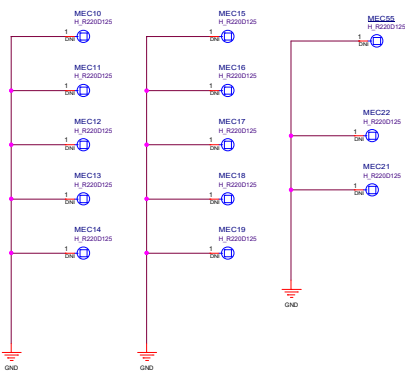
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劉魏  
weistang(唐浩健)  
(30001789)  
RMA工程課

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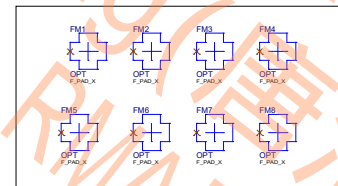
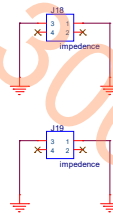
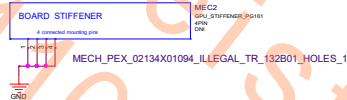
Mechanical: Mounting holes



Mechanical Holes Symbol

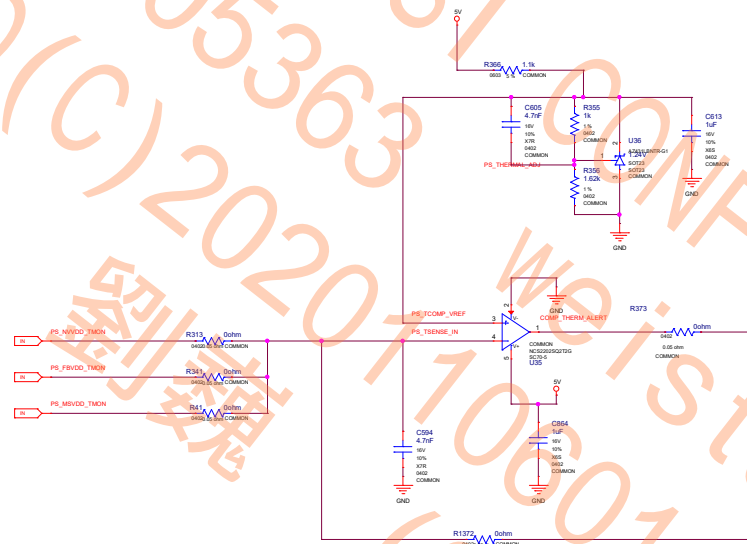


BACK STIFFENER:




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## VR THERMAL PROTECTION



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PCI TERM

